Search History

STN
(HCAPLUS, INSPEC, JAPIO, USPATFULL, INPADOC)
6/6/2007

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=> d his

     (FILE 'HOME' ENTERED AT 11:54:41 ON 06 JUN 2007)

     FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT
     11:55:27 ON 06 JUN 2007
L1         46972 S (CZ OR CZOCHRALSKI)
L2        566231 S (SINGLE OR MONO)(8A)(CRYSTAL# OR BOULE# OR INGOT#)
L3            24 S (N(W)REGION#)(8A)(ENTIRE(4A)PLANE)
L4        191397 S (RADIAL(W)DIRECTION#)
L5           112 S (14(2W)PPMA)
L6       1135308 S (MAGNET?)(8A)(FIELD# OR AREA# OR SURFACE#)

=> s l1 and l2 and l4 and l6
L7           127 L1 AND L2 AND L4 AND L6

=> s l3 and l7
L8             9 L3 AND L7

=> d l8 1-9 abs,bib

L8   ANSWER 1 OF 9  USPATFULL on STN
AB     The present invention is a method for producing a single
       crystal in accordance with Czochralski method by
       flowing an inert gas downward in a chamber 1 of a single
       crystal-pulling apparatus 11 and surrounding a single
       crystal 3 pulled from a raw material melt 2 with a gas
       flow-guide cylinder 4, wherein when a single crystal
       within N region outside OSF region generated in a ring shape in the
       radial direction of the single
       crystal is pulled, the single crystal within
       N region is pulled in a condition that flow amount of the inert gas
       between the single crystal and the gas flow-guide
       cylinder is 0.6 D(L/min) or more and pressure in the chamber is 0.6
       D(hPa) or less, in which D (mm) is a diameter of the single
       crystal to be pulled. It is preferable that there is used the
       gas flow-guide cylinder that Fe concentration is 0.05 ppm or less, at
       least, in a surface thereof. Thereby, there is provided a method for
       producing a single crystal, wherein in the case that
       a single crystal is produced by an apparatus having
       a gas flow-guide cylinder in accordance with CZ method, the
       single crystal has low defect density and Fe
       concentration can be suppressed to be 1+10.sup.10 atoms/cm.sup.3
       or less even in a peripheral part thereof.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN     2006:277991  USPATFULL
TI     Process for producing single crystal and silicon
       crystal wafer
IN     Fusegawa, Izumi, Fukushima, JAPAN
       Mitamuria, Nobuaki, Fukushima, JAPAN
       Yanagimachi, Takahiro, Fukushima, JAPAN
PA     Shin-Etsu Handotai Co., Ltd., Chiyoda-ku, JAPAN (non-U.S. corporation)
PI     US 2006236919       A1  20061026
AI     US 2004-568186      A1  20040813 (10)
       WO 2004-JP11685         20040813
                               20060303  PCT 371 date
PRAI   JP 2003-296837      20030820
DT     Utility
FS     APPLICATION
LREP   OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320, US
CLMN   Number of Claims: 18
ECL    Exemplary Claim: 1-6
DRWN   5 Drawing Page(s)
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5

LN.CNT 631
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 2 OF 9 USPATFULL on STN
AB An SOI wafer in which a base wafer and a bond wafer respectively consisting of silicon single crystal are bonded via an oxide film, and then the bond wafer is thinned to form a silicon active layer, wherein the base wafer is formed of silicon single crystal grown by Czochralski method, and the whole surface of the base wafer is within N region outside OSF region and doesn't include a defect region detected by Cu deposition method, or the whole surface of the base wafer is within a region outside OSF region, doesn't include a defect region detected by Cu deposition method, and includes I region containing dislocation cluster due to interstitial silicon. Thereby, there is provided an SOI wafer that retains high insulating properties and has an excellent electrical reliability in device fabrication even in the case of forming an extremely thin interlevel dielectric oxide film with, for example, a thickness of 100 nm or less.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2006:135027 USPATFULL
TI Soi wafer and production method therefor
IN Sakurada, Masahiro, Fukushima, JAPAN
Mitamura, Nobuaki, Fukushima, JAPAN
Fusegawa, Izumi, Fukushima, JAPAN
PA SHIN-ETSU HANDOTAI CO., LTD., TOKYO, JAPAN (non-U.S. corporation)
PI US 2006113594 A1 20060601
AI US 2004-542376 A1 20040122 (10)
WO 2004-JP547 20040122
20050714 PCT 371 date
PRAI JP 2003-15396 20030123
JP 2003-15072 20030123
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320, US
CLMN Number of Claims: 11
ECL Exemplary Claim: 1-6
DRWN 12 Drawing Page(s)
LN.CNT 1034
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 3 OF 9 USPATFULL on STN
AB In a method for producing an SOI wafer comprising steps of implanting hydrogen ions etc. from a surface of a bond wafer 21 to form an ion-implanted layer 24 inside the wafer, bonding the ion-implanted surface of the bond wafer and a surface of a base wafer 22 via an oxide film 23 or directly, and forming an SOI wafer by delaminating a part of the bond wafer at the ion-implanted layer by heat treatment, wherein a silicon wafer consisting of silicon single crystal grown by Chochralski method, which is occupied by N region outside OSF generated in a ring shape and has no defect region detected by Cu deposition method, is used as the bond wafer. Thereby, even in the case of forming an extremely thin SOI layer 27 such that, for example, its thickness is 200 nm or less, there is provided an SOI wafer which has an excellent electric property without causing micro pits by cleaning with hydrofluoric acid etc., and in addition, can be produced without increasing the number of process.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:75335 USPATFULL
TI Soi wafer and method for manufacturing soi wafer
IN Sakurada, Masahiro, Fukushima, JAPAN
Mitamura, Nobuaki, Fukushima, JAPAN

Fusegawa, Izumi, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
PI US 2005064632 A1 20050324
US 7129123 B2 20061031
AI US 2004-500580 A1 20040701 (10)
WO 2003-JP13645 20031024
PRAI JP 2002-217634 20021031
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320
CLMN Number of Claims: 14
ECL Exemplary Claim: CLM-01-13
DRWN 9 Drawing Page(s)
LN.CNT 719
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 4 OF 9 USPATFULL on STN
AB A silicon single crystal wafer grown by the CZ method, which is doped with nitrogen and has an N-region for the entire plane and an interstitial oxygen concentration of 8 ppma or less, or which is doped with nitrogen and has an interstitial oxygen concentration of 8 ppma or less, and in which at least void type defects and dislocation clusters are eliminated from the entire plane, and a method for producing the same. Thus, there are provided a defect-free silicon single crystal wafer having an N-region for the entire plane, in which void type defects and dislocation clusters are eliminated, produced by the CZ method under readily controllable stable production conditions with a wide controllable range, and a method producing the same.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:13194 USPATFULL
TI Silicon single crystal wafer and production method thereof and soi wafer
IN Iida, Makoto, Gunma, JAPAN
Kimura, Masanori, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6843847 B1 20050118
WO 2001036719 20010525
AI US 2001-869912 20010709 (9)
WO 2000-JP7809 20001107
20010709 PCT 371 date
PRAI JP 1999-322487 19991112
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 21
ECL Exemplary Claim: 1
DRWN 2 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 884
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 5 OF 9 USPATFULL on STN
AB A silicon single crystal wafer for epitaxial growth grown by the CZ method, which is doped with nitrogen and has a V-rich region over its entire plane, or doped with nitrogen, has an OSF region in its plane, and shows an LEP density of 20/cm.sup.2 or less or an OSF density of 1+10.sup.4/cm.sup.2 or less in the OSF region, epitaxial wafer utilizing the substrate, as well as methods for producing them and method for evaluating a substrate suitable for an epitaxial wafer. There are provided a substrate for an epitaxial wafer that suppresses crystal defects to be generated in an epitaxial layer

when epitaxial growth is performed on a CZ silicon single crystal wafer doped with nitrogen and also has superior IG ability, epitaxial wafer utilizing the substrate, as well as methods for producing them and method for evaluating a substrate suitable for an epitaxial wafer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:102116 USPATFULL
TI Silicon single crystal wafer for epitaxial wafer, epitaxial wafer, and methods for producing the same and evaluating the same
IN Kimura, Akihiro, Gunma, JAPAN
Iida, Makoto, Gunma, JAPAN
Hayamizu, Yoshinori, Gunma, JAPAN
Aihara, Ken, Gunma, JAPAN
Kimura, Masanori, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6548035 B1 20030415
WO 2001027362 20010419
AI US 2001-868058 20010614 (9)
WO 2000-JP6965 20001005
PRAI JP 1999-294523 19991015
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 925
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 6 OF 9 USPATFULL on STN
AB A silicon wafer obtained by slicing a silicon single crystal ingot grown by the Czochralski method with or without nitrogen doping, wherein the silicon wafer has an NV-region, an NV-region containing an OSF ring region or an OSF ring region for its entire plane and has an interstitial oxygen concentration of 14 ppma or less, and a method for producing it, as well as a method for evaluating defect regions of a silicon wafer. Thus, there are provided a silicon wafer that stably provides oxygen precipitation regardless of position in crystal or device production process, and a method for producing it. Further, defect regions of a silicon wafer of which pulling conditions are unknown and thus of which defect regions are also unknown can be evaluated.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:95797 USPATFULL
TI Silicon wafer and production method thereof and evaluation method for silicon wafer
IN Takeno, Hiroshi, Gunma, JAPAN
Shigeno, Hideki, Gunma, JAPAN
Iida, Makoto, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6544490 B1 20030408
WO 2001036718 20010525
AI US 2001-869932 20010709 (9)
WO 2000-JP7808 20001107
PRAI JP 1999-322242 19991112
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 11

ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 906
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 7 OF 9 USPATFULL on STN
AB A method for producing a silicon single crystal, wherein, when a silicon single crystal is grown by the Czochralski method, the crystal is pulled with such conditions as present in a region defined by a boundary between a V-rich region and an N-region and a boundary between an N-region and an I-rich region in a defect distribution chart showing defect distribution which is plotted with D [mm] as abscissa and F/G [mm.sup.2/° C..multidot.min] as ordinate, wherein D represents a distance between center of the crystal and periphery of the crystal, F/G [mm/min] represents a pulling rate and G [° C./mm] represents an average temperature gradient along the crystal pulling axis direction in the temperature range of from the melting point of silicon to 1400° C., and time required for crystal temperature to pass through the temperature region of from 900° C. to 600° C. is controlled to be 700 minutes or shorter, and a silicon single crystal wafer grown by the Czochralski method, which is a silicon single crystal wafer having N -region for its entire plane, and does not generate OSFs by a single-step thermal oxidation treatment, but generates OSFs by a two-step thermal oxidation treatment. According to the method, a silicon single crystal wafer of an extremely low defect density, which has the N-region for the entire plane of the crystal, is obtained by the CZ, while maintaining high productivity.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:815 USPATFULL
TI Single-crystal silicon wafer having few crystal defects and method for manufacturing the same
IN Iida, Makoto, Annaka, JAPAN
Kimura, Masanori, Annaka, JAPAN
Muraoka, Shozo, Annaka, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6334896 B1 20020101
WO 2000031324 20000602
AI US 2000-600033 20000711 (9)
WO 1999-JP6287 19991111
20000711 PCT 371 date
PRAI JP 1998-329309 19981119
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 738
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 8 OF 9 USPATFULL on STN
AB There is disclosed a method for producing a silicon single crystal by growing the silicon single crystal by the Czochralski method, characterized in that the crystal is pulled at a pulling rate [mm/min] within a range of from V1 to V1+0.062+G while the crystal is doped with nitrogen during the growing, where G [K/mm] represents an average temperature gradient along the crystal growing direction, which is for a temperature range of from the melting point of silicon to 1400° C., and provided in an

apparatus used for the crystal growing, and V1 [mm/min] represents a pulling rate at which an OSF ring disappears at the center of the crystal when the crystal is pulled by gradually decreasing the pulling rate. The method of the present invention can produce silicon single crystal wafers exhibiting an extremely low defect density over the entire plane of the crystal, in particular, with no small pits, and having an excellent oxide dielectric breakdown voltage, based on the CZ method under widely and easily controllable production conditions at a high production rate and high productivity.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:32607 USPATFULL
TI Method for producing low defect silicon single crystal doped with nitrogen
IN Iida, Makoto, Gunma-ken, Japan
Tamatsuka, Masaro, Gunma-ken, Japan
Kusaki, Wataru, Gunma-ken, Japan
Kimura, Masanori, Gunma-ken, Japan
Muraoka, Shozo, Gunma-ken, Japan
PA Shin-Etsu Handotai Co., Ltd., Tokyo, Japan (non-U.S. corporation)
PI US 6197109 B1 20010306
AI US 1999-329615 19990610 (9)
PRAI JP 1998-188227 19980618
DT Utility
FS Granted
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Hogan & Hartson, LLP.
CLMN Number of Claims: 8
ECL Exemplary Claim: 1
DRWN 3 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 748
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 9 OF 9 USPAT2 on STN
AB In a method for producing an SOI wafer comprising steps of implanting ions from a bond wafer surface to form an ion-implanted layer inside the wafer, bonding the ion-implanted bond wafer surface and a surface of a base wafer via an oxide film or directly, and forming an SOI wafer by delaminating by heat treatment a part of the bond wafer at the ion-implanted layer, the bond wafer is a silicon wafer that consists of a silicon single crystal grown by Czochralski method, that is occupied by N region outside OSF generated in a ring shape and that has no defect region detected by Cu deposition method. Thereby, even an extremely thin SOI layer having a thickness of 200 nm or less, can provide an SOI wafer that has an excellent electric property without micro pits caused by acid cleaning, and can be produced without increasing the number of processes.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:75335 USPAT2
TI SOI wafer and a method for producing an SOI wafer
IN Sakurada, Masahiro, Fukushima, JAPAN
Mitamura, Nobuaki, Fukushima, JAPAN
Fusegawa, Izumi, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 7129123 B2 20061031
WO 2004040650 20040513
AI US 2003-500580 20031024 (10)
WO 2003-JP13645 20031024
20040701 PCT 371 date
RLI Continuation of Ser. No. US 2002-204935, filed on 27 Aug 2002, Pat. No. US 6913646

PRAI JP 2002-317634 20021031
DT Utility
FS GRANTED
EXNAM Primary Examiner: Lee, Calvin
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 716
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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Day : Wednesday

PALM INTRANET

Date: 6/6/2007
Time: 12:04:45

Inventor Name Search Result

Your Search was:

Last Name = IIDA
First Name = MAKOTO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
05810759	4163215	150	06/28/1977	SAFETY LOCK SYSTEM	IIDA, MAKOTO
05895605	4227577	150	04/12/1978	FIRE-EXTINGUISHING SYSTEM	IIDA, MAKOTO
06336323	4409341	150	12/31/1981	COMPOSITION FOR FIRE RETARDANT URETHANE FOAM	IIDA, MAKOTO
06880012	4734448	150	06/30/1986	PROPYLENE POLYMER COMPOSITION	IIDA, MAKOTO
07219267	Not Issued	166	07/15/1988	ELECTROCONDUCTIVE RESIN COMPOSITION FOR MOLDING AND ELECTROMAGNETIC WAVE INTERFERENCE SHIELD STRUCTURE MOLDED FROM THE COMPOSITION	IIDA, MAKOTO
07538113	5071223	150	06/14/1990	CIRCUIT STRUCTURE FORMED BY INSERT MOLDING OF ELECTRIC AND/OR OPTICAL TRANSMISSION MEDIUM	IIDA, MAKOTO
07592545	Not Issued	166	10/02/1990	FOCUS DRAW-IN METHOD FOR OPTICAL DISC DEVICE	IIDA, MAKOTO
07769348	6156427	250	10/02/1991	ELECTROCONDUCTIVE RESIN COMPOSITION FOR MOLDING AND ELECTROMAGNETIC WAVE INTERFERENCE SHIELD STRUCTURE MOLDED FROM THE COMPOSITION	IIDA, MAKOTO
07785000	5179601	150	10/30/1991	METHOD OF MANUFACTURING CIRCUIT STRUCTURE BY INSERT MOLDING OF ELECTRIC AND/OR OPTICAL TRANSMISSION MEDIUM	IIDA, MAKOTO

07866166	Not Issued	166	06/29/1992	OPTICAL DISK SYSTEM	IIDA, MAKOTO
07939045	Not Issued	166	09/03/1992	FOCUS DRAW-IN SYSTEM FOR OPTICAL DISC DEVICE	IIDA, MAKOTO
08137211	5414682	150	10/18/1993	FOCUS DRAW-IN SYSTEM FOR OPTICAL DISC DEVICE	IIDA, MAKOTO
08172413	5491301	150	12/22/1993	SHIELDING METHOD AND CIRCUIT BOARD EMPLOYING THE SAME	IIDA, MAKOTO
08279318	5461599	150	07/22/1994	OPTICAL DISK SYSTEM	IIDA, MAKOTO
08809295	Not Issued	161	03/27/1997	PROPYLENE RESIN COMPOSITION FOR AUTOMOTIVE INTERIOR PARTS, AND AUTOMOTIVE INTERIOR PARTS	IIDA, MAKOTO
08827060	Not Issued	161	03/26/1997	PRESS WORKING METHOD AND EQUIPMENT THEREFOR	IIDA, MAKOTO
08915397	5871578	150	08/20/1997	METHODS FOR HOLDING AND PULLING SINGLE CRYSTAL	IIDA, MAKOTO
08923963	5911821	150	09/05/1997	METHOD OF HOLDING A MONOCRYSTAL, AND METHOD OF GROWING THE SAME	IIDA, MAKOTO
08929670	5964941	150	09/15/1997	CRYSTAL PULLING METHOD AND APPARATUS	IIDA, MAKOTO
08944869	5882397	150	10/06/1997	CRYSTAL PULLING METHOD	IIDA, MAKOTO
09039830	6053975	150	03/16/1998	CRYSTAL HOLDING APPARATUS	IIDA, MAKOTO
09101941	6120749	150	07/17/1998	SILICON SINGLE CRYSTAL WITH NO CRYSTAL DEFECT IN PERIPHERAL PART OF WAFER AND PROCESS FOR PRODUCING THE SAME	IIDA, MAKOTO
09109530	5968264	150	07/02/1998	METHOD AND APPARATUS FOR MANUFACTURING A SILICON SINGLE CRYSTAL HAVING FEW CRYSTAL DEFECTS, AND A SILICON SINGLE CRYSTAL AND SILICON WAFERS MANUFACTURED BY THE SAME	IIDA, MAKOTO
09140288	5948164	250	08/25/1998	SEED CRYSTAL HOLDER	IIDA, MAKOTO

09173931	6027562	150	10/16/1998	METHOD FOR PRODUCING A SILICON SINGLE CRYSTAL HAVING FEW CRYSTAL DEFECTS, AND A SILICON SINGLE CRYSTAL AND SILICON WAFERS PRODUCED BY THE METHOD	IIDA, MAKOTO
09188490	6066306	150	11/09/1998	SILICON SINGLE CRYSTAL WAFER HAVING FEW CRYSTAL DEFECTS, AND METHOD FOR PRODUCING THE SAME	IIDA, MAKOTO
09194232	6445872	150	11/23/1998	RECORDING AND REPRODUCING APPARATUS FOR RECORDING DIGITAL BROADAST COMPRESSION-CODED DATA T OF VIDEO SIGNALS OF A MULTIPLICITY OF CHANNELS	IIDA, MAKOTO
09197130	6048395	150	11/20/1998	METHOD FOR PRODUCING A SILICON SINGLE CRYSTAL HAVING FEW CRYSTAL DEFECTS	IIDA, MAKOTO
09264514	6191009	150	03/08/1999	METHOD FOR PRODUCING SILICON SINGLE CRYSTAL WAFER AND SILICON SINGLE CRYSTAL WAFER	IIDA, MAKOTO
09294323	6191675	150	04/20/1999	HIGH VOLTAGE TRANSFORMER AND IGNITION TRANSFORMER USING THE SAME	IIDA, MAKOTO
09313856	6299982	150	05/18/1999	SILICON SINGLE CRYSTAL WAFER AND METHOD FOR PRODUCING SILICON SINGLE CRYSTAL WAFER	IIDA, MAKOTO
09318055	6077343	150	05/25/1999	SILICON SINGLE CRYSTAL WAFER HAVING FEW DEFECTS WHEREIN NITROGEN IS DOPED AND A METHOD FOR PRODUCING IT	IIDA, MAKOTO
09329615	6197109	150	06/10/1999	METHOD FOR PRODUCING LOW DEFECT SILICON SINGLE CRYSTAL DOPED WITH NITROGEN	IIDA, MAKOTO
09359078	6159438	150	07/22/1999	METHOD AND APPARATUS FOR MANUFACTURING A	IIDA, MAKOTO

				SILICON SINGLE CRYSTAL HAVING FEW CRYSTAL DEFECTS, AND A SILICON SINGLE CRYSTAL AND SILICON WAFERS MANUFACTURED BY THE SAME	
09454841	6120599	150	12/06/1999	SILICON SINGLE CRYSTAL WAFER HAVING FEW CRYSTAL DEFECTS, AND METHOD FOR PRODUCING THE SAME	IIDA, MAKOTO
09459849	6120598	150	12/13/1999	METHOD FOR PRODUCING A SILICON SINGLE CRYSTAL HAVING FEW CRYSTAL DEFECTS, AND A SILICON SINGLE CRYSTAL AND SILICON WAFERS PRODUCED BY THE METHOD	IIDA, MAKOTO
09492001	6348180	150	01/26/2000	SILICON SINGLE CRYSTAL WAFER HAVING FEW CRYSTAL DEFECTS	IIDA, MAKOTO
09572788	6780067	150	05/17/2000	COMBINED INTEGRAL MOLDED PRODUCT USING PRE-MOLDED MEMBER	IIDA, MAKOTO
09577252	6261361	150	05/19/2000	Silicon single crystal wafer having few defects wherein nitrogen is doped and a method for producing it	IIDA, MAKOTO
09600033	6334896	150	07/11/2000	SINGLE-CRYSTAL SILICON WAFER HAVING FEW CRYSTAL DEFECTS AND METHOD FOR MANUFACTURING THE SAME	IIDA, MAKOTO
09661985	6364947	150	09/14/2000	Method and apparatus for manufacturing a silicon single crystal Having few crystal defects, and a silicon single crystal and silicon wafers manufactured by the same	IIDA, MAKOTO
09828206	6401643	250	04/09/2001	SEWN COVER ASSEMBLY AND PRODUCT FOAMED THEREWITH	IIDA, MAKOTO
09830386	6544332	150	04/26/2001	METHOD FOR MANUFACTURING SILICON SINGLE CRYSTAL, SILICON SINGLE CRYSTAL	IIDA, MAKOTO

				MANUFACTURED BY THE METHOD, AND SILICON WAFER	
09868058	6548035	150	06/14/2001	SILICON SINGLE CRYSTAL WAFER FOR EPITAXIAL WAFER, EPITAXIAL WAFER, AND METHODS FOR PRODUCING THE SAME AND EVALUATING THE SAME	IIDA, MAKOTO
09869912	6843847	150	07/09/2001	SILICON SINGLE CRYSTAL WAFER, METHOD FOR PRODUCING THE SAME AND SOI WAFER	IIDA, MAKOTO
09869932	6544490	150	07/09/2001	SILICON WAFER AND PRODUCTION METHOD THEREOF AND EVALUATION METHOD FOR SILICON WAFER	IIDA, MAKOTO
09884784	Not Issued	161	06/19/2001	Hybrid housing of metal board and synthetic resin	IIDA, MAKOTO
09936920	6599360	150	09/20/2001	SILICON WAFER, METHOD FOR DETERMINING PRODUCTION CONDITIONS OF SILICON SINGLE CRYSTAL AND METHOD FOR PRODUCING SILICON WAFER	IIDA, MAKOTO
10009910	Not Issued	124	12/12/2001	Silicon wafer, silicon epitaxial wafer, anneal wafer and method for producing them	IIDA, MAKOTO
10130431	6841450	150	05/17/2002	ANNEALED WAFER MANUFACTURING METHOD AND ANNEALED WAFER	IIDA, MAKOTO

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Search Another: Inventor **Last Name** Iida **First Name** Makoto Search

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